A 110 nA PACEMAKER SENSING CHANNEL IN CMOS ON SILICON-ON-INSULATOR

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ABSTRACT

The design of a sensing channel for implantable cardiac pacemakers in CMOS on Silicon-on-Insulator (SOI) technology is presented. The total current consumption is lowered to only 110nA thanks to the optimization at the architectural level, the application of a new class AB design approach at the operational transconductance amplifier (OTA) and the exploitation of the improved characteristics of thin-film fully depleted SOI CMOS technology. The core of the prototyped sense channel (OTA and comparator) occupies 0.06mm^2 in a 3μm technology and is suitable for operation from implantable grade batteries with power supply voltages from 2.8V down to 2V. Experimental results of the building blocks and complete sensing channel performance are presented. The achieved results demonstrate the benefits of fully depleted SOI CMOS technology for micropower applications.

1. INTRODUCTION

Cardiac pacemakers remain the main implantable medical device. A cardiac pacemaker reestablishes a normal rhythm to a diseased heart that presents a slower contraction rate. This is achieved by provoking the heart contraction through an electrical stimulus. To the basic function of stimulating the heart, modern pacemakers add several features such as a detection of the spontaneous contraction of the heart, a telemetry link to receive programmable parameters and send status and statistics data, battery voltage measurement and methods for sensing physical activity (usually by means of an accelerometer) in order to adapt the heart rate accordingly. Though this trend has been possible due to the evolution of microelectronic systems, the reduction of power consumption (to increase the device lifetime) and size (which is linked to consumption through the battery size) are still central goals in the framework of these increased capabilities.

The circuit that processes the bioelectric signals present in the cardiac muscle to detect spontaneous cardiac activity is known as sense amplifier or sensing channel. This circuit must be active during most part (around 70% to 80%) of the cardiac cycle and the so-called "dual chamber" pacemakers, which interact with both the upper (atria) and lower (ventricles) chambers of the heart, require two of these circuits. Typical figures for the consumption of each of these blocks is around 1μA [1], which accounts for 10 to 20 % of the total pacemaker consumption. Besides its significance in the particular application of a pacemaker, this block, though simple, is a representative example of implantable biomedical analog block.

This paper presents the design and test of a ultra low power implementation of a sensing channel circuitry. A major power reduction is achieved by the joint application of a simple architecture with power saving building blocks and the superior characteristics of fully depleted Silicon-on-Insulator (SOI) CMOS technology.

The paper is organized as follows. Section 2 describes the circuit requirements and the overall selected architecture. It is then discussed how a power oriented design leads to our optimal solution. In Section 3 the main characteristics of the building blocks (OTA and comparator) are presented. Section 4 shows the experimental results on the performance of the whole circuit. Finally, section 5 summarizes the main results and conclusions.

2. SENSE CHANNEL REQUIREMENTS AND ARCHITECTURE

The detection of the electrical activity of the heart requires amplification / filtering and comparison to determine if a heart beat has occurred. A standard test waveform representing the cardiac signal is a triangular wave with 2ms rise time and 13ms fall time [2]. Typical thresholds of detection are amplitudes from 0.2mV to 3.2mV in the

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atrium and 0.4mV to 6.4mV in the ventricle. Though the energy of intracardiac signals have significant components at lower frequencies [3], a frequency passband from 70Hz to 200Hz and 20 dB/dec roll-off on both sides has been proved, in several generations of pacemakers, to be a suitable choice that leaves the electrical network 50 and 60Hz fundamentals out of the band while allowing the correct detection of physiological signals. This circuit is powered from the usual power supply of implantable devices, a Lithium-Iodine battery, with 2.8V full charge voltage. In order to guarantee operation during an acceptable time from the detection of the battery low condition to its replacement, the circuit must be fully operative for supply voltages down to 2.0V.

The threshold of detection must be variable to adapt the operation to the characteristics of each patient. The main alternatives are to have a variable gain amplifier and a fixed comparison threshold or a fixed gain amplifier with a variable comparison threshold. We selected the second alternative, where, as described in [4] for a bulk CMOS implementation, the variable threshold is appropriately implemented through a capacitive charge redistribution D/A converter. This capacitive D/A converter can be refreshed once per cardiac cycle when the sense amplifier is not active, and as its output is basically constant, the power consumption is absolutely negligible. To have 16 programming steps for the sensitivity of the circuit, the central 16 levels of a 5 bits D/A with full scale equal to the supply voltage can be used as in [4]. This avoids operation close to the supply rails for the input stage of the comparator and the output stage of the amplifier. In this case, each threshold step at the input of the comparator is the power supply over 32, i.e. 87.5mV at nominal supply voltage. In order to allow detection of input test signals of 0.2mV amplitude with this threshold, the band-pass filter must have an in-band maximum gain of about 660.

The basic architecture is shown in Fig. 1. Depending on overall system decisions, variations on this structure can be applied, like having a differential input or second comparator to have a window comparator.

The resistances and capacitances shown in Fig. 1 are implemented off-chip. R1, C1 define the 70Hz high-pass characteristic, while the 200 Hz low pass characteristic can be defined by the OTA first order roll-off, adjusted through C2 if needed. This implementation, although it requires some external components and must cope with high off-chip capacitances, can achieve extremely low power consumption thanks to its simplicity, when compared to switched-capacitor or integrated continuous-time filters that require extra power in either antialias filtering and clock generation or on-chip self-tuning schemes. Furthermore, depending on the overall system implementation, since the inputs of this circuit are directly in contact with the heart, some of these external

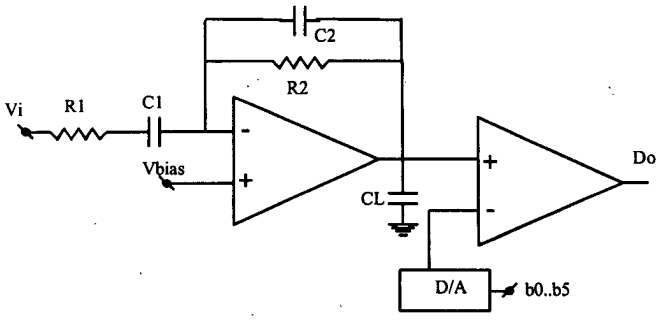

Fig. 1: Basic Sense Channel Architecture

components, as C1, might nevertheless be required to provide redundant protection against faults that might be risky for the patient, such as the flow of direct current through the heart.

The power consumption of the circuit was drastically reduced by optimization at the specification, circuit and technological implementation levels. At the specification level, the requirements on the frequency response of the OTA were optimized for the intended application. At the circuit level, a new class AB OTA output stage design approach was applied. Finally at the technological level, a thin-film fully-depleted SOI CMOS process was applied.

The main characteristics of this SOI process are lower parasitic capacitances, lower leakage, quasi-ideal subtreshold slope which allows for a lower threshold voltage with acceptable off currents values and allows to reach higher transconductance to current ratios [5]. In this particular process, when operating with 2.8V supply voltage and substrate (back gate) voltage at half the supply voltage, the threshold voltage is 0.5V for both n and p type transistors.

Class AB OTA and comparator experimental prototypes were designed, fabricated and tested. The following sections summarize the main design decisions and results concerning each of the modules and the overall experimental results for the whole sense channel.

3. A 90 nA CLASS AB OTA AND A 20 nA COMPARATOR

Class AB amplifiers contribute to minimize power by several ways; on one hand by decoupling the large signal (i.e. slew rate) and small signal (i.e. stability) requirements on the output stage; on the other hand by reducing quiescent current consumption when the signal to be processed, as in this case the cardiac signal, is "active" during only a small part of the system cycle. A class AB architecture will suit this kind of application if it can achieve very low-power consumption and low-voltage operation with an accurate control of the quiescent current over all the power supply voltage range.

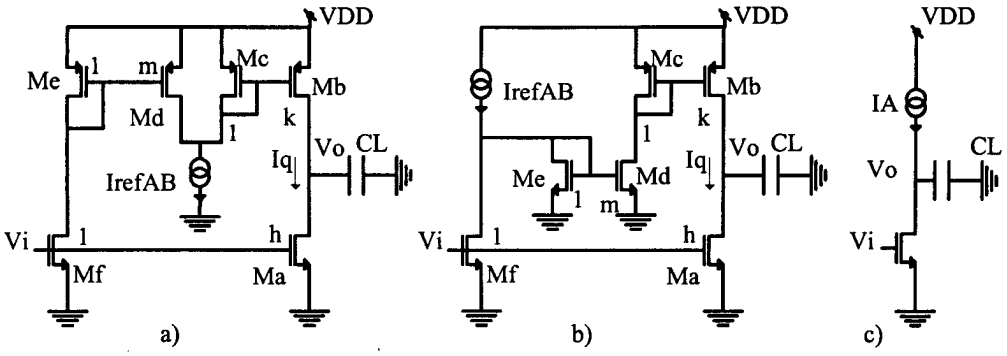

Fig. 2. Class AB output stages (a, b) and conventional class A output stage (c).

The proposed class AB design approach achieves a superior bandwidth to consumption ratio due to a very simple structure and the application of a transconductance multiplication effect [6]. The considered output stages are simple class AB common-source structures as shown in Figs. 2.a and 2.b. The structure of Fig 2.b has been applied previously, as in [7] and [8], though not exploiting the principle applied here. In our case a significant reduction in power consumption is achieved by two means. Firstly the architecture provides a low impedance path from the input of the driver stage to the output transistors, avoiding compensation capacitors. Secondly the output stage transconductance (gm) is boosted through the current mirrors gain resulting in a significant improvement of the transconductance to current ratio (gm/ID) of the output stage. Multiplication factors as high as 25 in gm and 12 in gm/ID can be achieved while assuring stability [6]. Although primarily conceived in the framework of the pacemaker application, the proposed circuit architecture has general application and in [6] we present various realizations reaching transition frequencies up to 10MHz.

We applied the output stage of Fig. 2.b as the second stage of a Miller amplifier, where the Miller capacitance is connected between the Vi and Vo terminals of Fig 2.b. Since this amplifier non-dominant pole is proportional to the second stage transconductance, we will be decreasing the second stage current in a proportion comparable to the increase in the second stage gm/ID ratio, when compared to the equivalent class A outputs stage (shown in Fig. 2.c) for similar stability requirements. The increase in gm/ID is however not completely translated into a decrease in current, because the non dominant pole must be slightly increased with respect to the class A case, to have the same phase margin while allowing the phase shift introduced by the current mirrors frequency response. Taking these factors into account, reductions of quiescent current by a factor of 3 to 4 with respect to the class A case are achievable. Finally, the circuit is very well suited to low-voltage operation because the output stage only requires one gate –source plus one source –drain voltage for operation and these are furthermore reduced since the lower current requirement related to the tranconductance multiplication effect allows MOS operation in weaker inversion. Another important feature of this output stage is that the quiescent current is accurately fixed by the reference current IrefAB.

When specifying the OTA performance, we also took care to optimize them for the intended application and save consumption in this way. In particular, since the OTA will be operated in a fixed feedback loop, there is no need to set a phase margin requirement at the transition frequency, i.e. for unity gain operation, but instead, we need a given phase margin for the specified gain configuration. Our design criterium was then to have the non-dominant pole at least 2 decades after the closed-loop dominant pole frequency (200 Hz), i.e. after 20kHz, for a 50pF load.

The main measured characteristics of the amplifier, at 2V power supply in a 3μm SOI technology are the following:

Total quiescent supply current	90 nA
Load capacitance	50 pF
Closed loop –3dB point for a gain of 21	11kHz
Phase Margin at –3dB point for a gain of 21	56°
Open loop DC gain (no load resistance)	> 80dB
Current mirrors gain factors k,h,m	7,2,3
Transconductance multiplication factor	11.5
Ratio of equivalent class A consumption over Class AB quiescent consumption	3.1
Die area	0.03mm^2

The comparator is easily implemented with a symmetrical OTA [9] followed by two inverters. The low threshold voltage of 0.5V of the SOI technology and operation in weak inversion allow to achieve the required input range (0.5V to 1.5V) when operating from a 2V power supply with this simple structure, instead of more complex and power hungry rail to rail structures that are required to achieve this input range in standard Bulk CMOS technologies [4]. The measured characteristics of the comparator are: 30.5microsecs delay with a 100mV

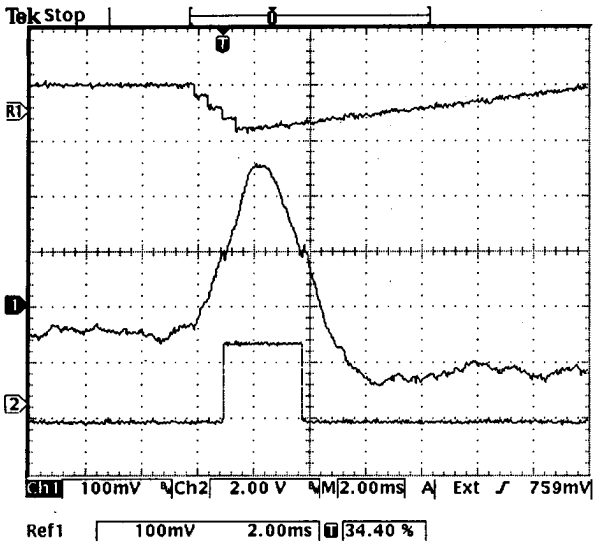

Fig. 3. Input signal (which is divided by a 201 factor, top), filter output (middle) and comparator output (bottom).

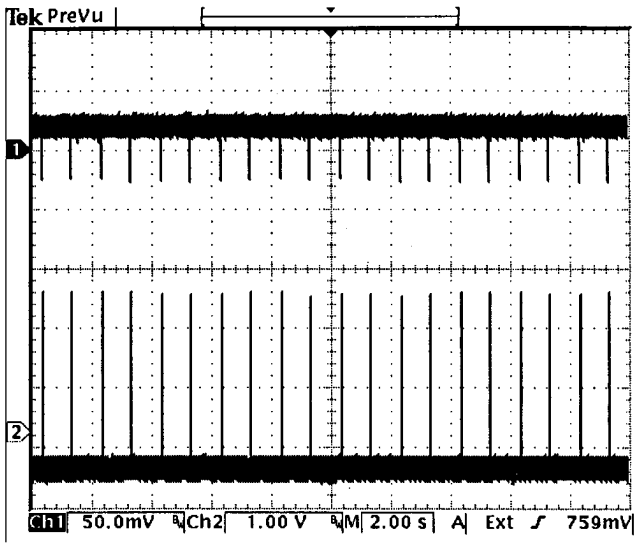

Fig. 4. Input signal (top) and comparator output (bottom).

step with 15mV overdrive and 12mV maximum offset in the 0.5V to 1.8V signal range with a 2V power supply.

4. SENSE CHANNEL EXPERIMENTAL RESULTS

Figs 3 and 4 show the experimental performance of the filter / amplifier and comparator structure of Fig. 1. In Fig. 3 the responses of the amplifier and comparator are shown when an input test signal of 0.4mV, which is the double of the minimum threshold amplitude, is applied. Fig. 4 shows how the circuit systematically detects an input test signal of the minimum threshold amplitude of 0.2mV. Measured output noise is 10.4mVrms.

5. CONCLUSIONS

The design and experimental test of pacemaker sense channel amplifier in CMOS on thin-film fully-depleted SOI technology have been presented. The application of a simple architecture with power efficient building blocks, like a class AB output stage which exploits transconductance multiplication based on current mirrors and the superior characteristics of fully-depleted Silicon-on-Insulator (SOI) technology allows to achieve a ultra low current consumption of 110nA.

6. ACKNOWLEDGEMENT

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